

SPECIFICATIONS

Document

Part Number: 97-04500-04 Revision A

10/20/17

MODEL NUMBER: R64093-127-10ADMDFS-A-F04

Control

Firmware: 47-04000-04

A Digital Frequency Synthesizer in a OEM Module with analog and digital modulation input and having up to a 15 watt RF output.

<u>PARAMETER</u>	<u>SPECIFICATION</u>
Total Bandwidth:	93-127 MHz
20MHz Segment Bandwidth:	93-113 MHz 100-120MHz 107-127 MHz
Clock Frequency:	1000 MHz
Step Size:	≤ 1 Hz with 30 Bits input
Frequency Settling Time:	310 ns maximum
Nominal Power Out:	10 Watts ± 10% over segment bandwidth
Maximum Power Out:	15 Watts ±10% over segment bandwidth
Harmonic Distortion: 2 nd :	-15 dBc maximum
3 rd :	-15 dBc maximum
Analog Modulation:	0 to +1 Volt Analog into 50 Ω, +1Volt = Full RF power output.
Digital Modulation:	TTL levels TTL High = Full RF output power TTL Low = Minimum RF output power No Signal = Full RF output power (pulled high internally)
Rise and Fall Time:	20 ns
Extinction Ratio:	
Digital:	30 dB minimum
Analog:	40 dB minimum
Reference Out:	A reference signal from the un-modulated output of the synthesizer. 0 dBm nominal
Applied Power:	+28 Volts DC @ 2 Amp maximum +3.3 Volts DC @ 1 Amp maximum
Outline Drawing	97-04500-04-15
MAXIMUM RATINGS:	
Ambient Temperature:	45° C
RF Output:	No DC Feedback
INPUT / OUTPUT CONNECTIONS:	
"FREQUENCY SELECT" Control	TTL 30 bit binary word, Digital Modulation Input, Reset, and a Latch control input through the 37 pin D sub connector. See page 2 for pinout.
+28V, +3.3V, and Gnd	Filtered Feedthrough
Mod In Analog	SMC Male
Reference Out	SMC Male
RF Output	SMA Female

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"FREQUENCY SELECT" PIN OUT
37-PIN MALE D-SUB CONNECTOR

<u>PIN</u>			<u>PIN</u>		
1	FS ₀	LSB	20	FS ₁	
2	FS ₂		21	FS ₃	
3	FS ₄		22	FS ₅	
4	FS ₆		23	FS ₇	
5	FS ₈		24	FS ₉	
6	FS ₁₀		25	FS ₁₁	
7	FS ₁₂		26	FS ₁₃	
8	FS ₁₄		27	FS ₁₅	
9	FS ₁₆		28	FS ₁₇	
10	FS ₁₈		29	FS ₁₉	
11	FS ₂₀		30	FS ₂₁	
12	FS ₂₂		31	FS ₂₃	
13	FS ₂₄		32	FS ₂₅	
14	FS ₂₆		33	FS ₂₇	
15	FS ₂₈		34	FS ₂₉	MSB
16	Latch		35	Digital Modulation Input (Active High)	
17	Master Reset (Active High)		36	Delta Frequency Latch	
18	N/C		37	N/C	
19	Ground				

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CONTROL WORD CALCULATIONS

The output frequency and step size is a function of the clock rate and the FREQUENCY SELECT (FS) data. The output frequency can be calculated from the formula:

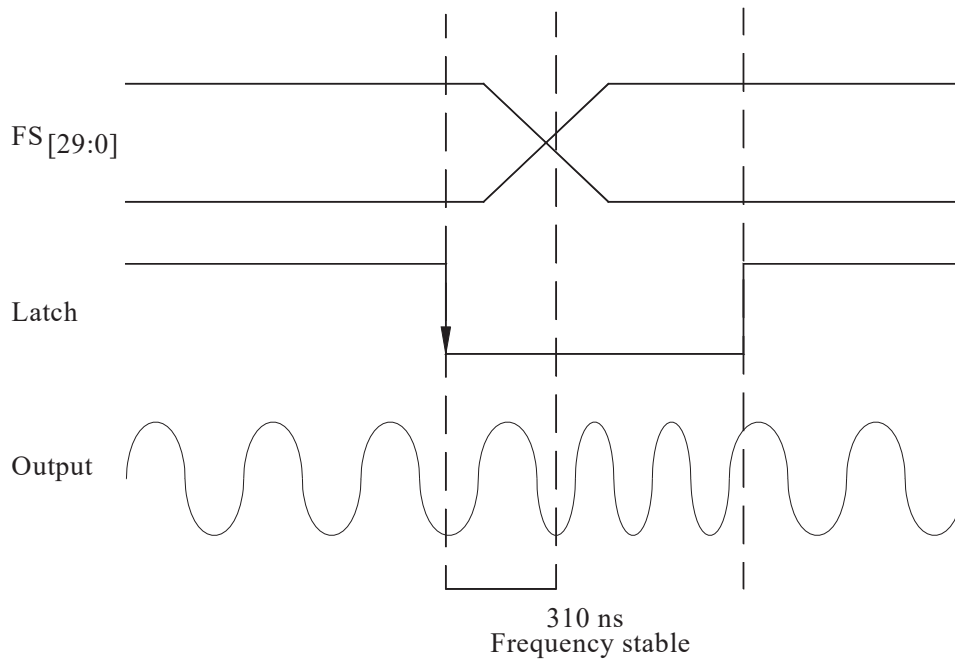
$$FS_{[29:0]} = \frac{F_{OUT} (2^{31})}{1000 \text{ MHz}} \quad \text{Where Fout is output frequency in MHz}$$

The LATCH function (pin 16) is a TTL compatible input which is used to load new frequency information into the driver. Frequency data is loaded into the driver when the signal on the LATCH pin goes from HIGH to LOW (falling edge).

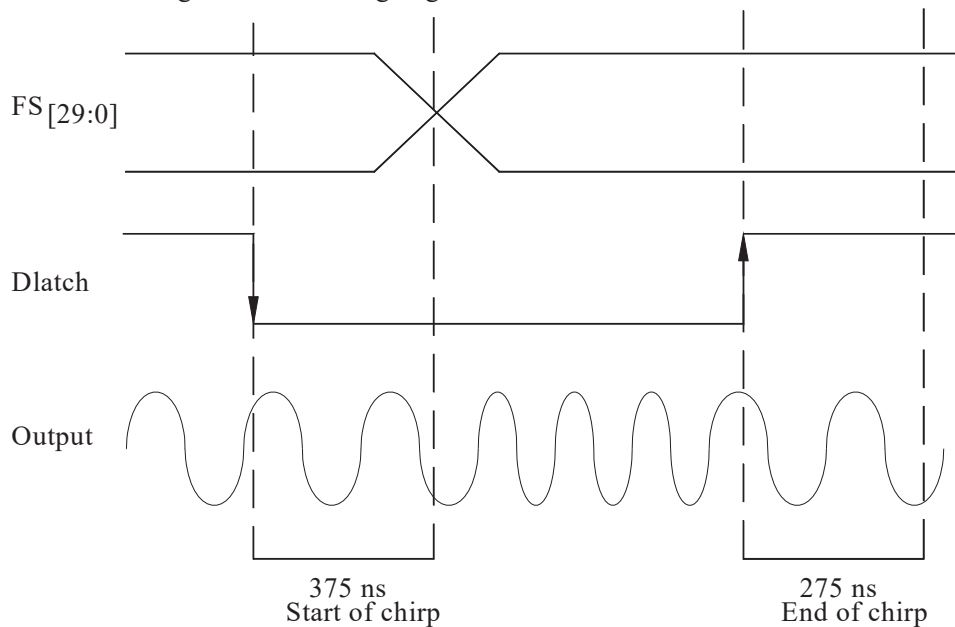
The DELTA FREQUENCY LATCH function (pin 36) is a TTL compatible input which is used to load new data frequency information into the driver. For Delta frequency word, the same calculation is used as the output frequency with negative values being entered in twos complement data is loaded on the falling edge.

Master RESET is a TTL active HIGH and resets the accumulator to zero, ie, no frequency output, when a TTL HIGH is applied to pin 17. This is pulled LOW via. a 1 K Ω resistor.

To generate a single frequency, apply the binary frequency word to the FS input, A falling edge on the LATCH input will then load the data and change the frequency.



To generate a frequency chirp, set the starting frequency as above and then apply the delta word to the FS input. A falling edge on DLATCH will then load the delta frequency word and initiate the chirp. The chirp will stop and output will return to starting value on a rising edge.



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As part of our policy of continuous product improvement we reserve the right to change specifications at any time.